Ferroelectricity in Hafnium Oxide: CMOS compatible Ferroelectric Field Effect Transistors

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Abstract

We report the discovery of ferroelectricity in crystalline hafnium silicon oxide. If HfO_2 based thin films, at a composition where the tetragonal phase is not yet stable, are crystallized in presence of a cap, the formation of an orthorhombic phase is observed. o-HfO_2 shows a piezoelectric response, while a polarization measurements exhibit a remanent polarization above 10 µC/cm² at a coercive field of 1 MV/cm, confirming this phase to be ferroelectric. Transistors fabricated with this material exhibit a permanent and switchable shift of the threshold voltage, allowing the realization of CMOS-compatible ferroelectric field effect transistors (FeFET) with sub 10 nm gate insulators for the first time.

Introduction

The FeFET is a long-term contender for a fast, low power and nonvolatile memory technology [1]. In these devices, information is permanently stored as polarization state of the gate insulator and can be read non-destructively as a shift of the threshold voltage. The FeFET concept was experimentally demonstrated decades ago [2], but the practical implementation has remained elusive. This is due to a thermodynamic incompatibility of known ferroelectrics, such as lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), and strained strontium titanate (STO) to silicon. Furthermore, due to low band offsets to silicon [4], thick films and noble metal electrode are required for low leakage devices. Numerous attempts have been made to improve the stability of ferroelectrics in contact with silicon by the introduction of buffer layers [3]. However, these approaches diminish the scalability of these devices as low EOT values are required for channel control in submicron devices. Furthermore, the introduction of an electrically thick buffer layer leads to a degradation of data retention due to a high depolarization field [5]. It becomes clear that a silicon compatible ferroelectric is a requirement for a reliable FeFET.

As known from the search for high-k gate dielectrics, only very few metal oxides are stable in contact to silicon and exhibit a sufficient band offset at the same time [6]. One of them is the well known high-k dielectric HfO_2, which has so far been only regarded as a paraelectric material.

It has been reported [7,8], that the properties of HfO_2, and consequently HfSiO, thin films can be influenced, if crystallized in presence of a cap. We investigated the influence of mechanical encapsulation on HfSiO thin films at lower Si content, where the complete stabilization of the tetragonal phase does not yet occur, in metal-insulator-metal capacitors.

Ferroelectricity in Silicon doped HfO_2

HfSiO was deposited by a metal organic atomic layer deposition process based on Tetrakis-(ethylmethylamino)-hafnium (TEMA-Hf), Tetrakis-dimethylamino-silane (4DMAS). metalorganic precursors and ozone. The silicon content was defined by varying the cycle ratio of the precursors and monitored by secondary ion mass spectrometry and elastic recoil detection analysis on samples without thermal treatment. The crystallization temperature of all films in the used thickness (7-12 nm) and composition range (2.5-6 mol% SiO_2) was above 500°C. Titanium nitride electrodes were deposited by a chemical vapor deposition process based on $TiCl_4$ and NH_3.

By lowering the deposition temperature of the titanium nitride (TiN) top electrode below the crystallization temperature of the HfSiO dielectric, it was possible to encapsulate amorphous films and induce the crystallization in a subsequent thermal treatment step above the crystallization temperature. We found that capacitors manufactured with this scheme exhibited non-linearities in their capacitance-voltage behavior, which did not occur if crystallization was induced prior to capping (Fig. 1). A comprehensive characterization was made by electrical polarization measurements on capped HfSiO films at different compositions. A gradual transition from ferroelectric to antiferroelectric polarization curves is observed with increasing silicon content (Fig. 2), which is also reflected in small signal capacitance-voltage measurements. Further evidence for ferroelectric and antiferroelectric behavior was obtained by measurement of the mechanic displacement (Fig. 3). The ferroelectric sample shows clear evidence of piezoelectric behavior, which is a prerequisite for ferroelectricity [9]. A symmetric, electrostrictive, response is observed for the antiferroelectric sample. This confirms that the observed polarization loops are not caused by parasitic electronic effects, but are of microstructural origin.

Since ferroelectricity is related to the crystal structure, a previously undetected crystalline phase must be present in the devices as prepared here. X-ray diffraction measurements (Fig. 4) of uncapped films show good agreement to a tetragonal/monoclinic-HfO_2 mixture, as it is commonly

observed for crystalline thin films. Capped samples, however, show a difraction pattern indicating a significant fraction of orthorhombic-HfO_2. The known forms of o-HfO_2 (Space groups Pbca and Pbcm) are centrosymmetric and therefore not ferroelectric. Furthermore, they are usually only observed at extremely high pressure. However, a similar diffraction pattern has been reported [10] for a rare orthorhombic phase with space group $Pbc2_1$ in Mg-doped ZrO_2, which emerged when the t→m transformation was inhibited by external stress in nano-scale crystallites. Similar conditions may arise in capped thin films of HfSiO (Fig. 5). Since the chemistry of ZrO_2 is almost identical to that of HfO_2, the same phases occur in both oxides. The $Pbc2_1$ space group is not centrosymmetric and does therefore not exclude ferroelectricity. A fuller account of our investigations of ferroelectric HfO_2 has been published in the meantime [11,12,13,14].

Ferroelectric Field Effect Transistors

The high bond strength of ferroelectric HfO_2 sets it apart from common ferroelectrics in several aspects: The high band gap and bad offsets allow for low leakage current even for very thin films below 10 nm. The excellent thermodynamic stability allows a direct contact to silicon and silicon dioxide. No noble metal electrodes or buffer layers are required as in earlier concepts [3].

Transistors were manufactured in a gate first scheme with a gate stack consisting of 1.2 nm thermal SiO_2 interface, 5-9 nm ferroelectric HfSiO insulator, and a TiN electrode. Crystallization of the HfSiO thin films was induced by a 1000 °C/20 s anneal in nitrogen after top electrode deposition. Both long and short channel devices were manufactured.

Fig. 6 compares the behavior of devices with ferroelectric and with antiferroelectric gate insulators during gate voltage sweeps and separate program and sense steps. The antiferroelectric device is dominated by charge trapping, as evident from a clockwise hysteresis and a threshold voltage (Vt) shift in direction of the programming bias. This behavior can be ascribed to trapping of electrons from the channel region, a well-known behavior for devices with crystalline HfSiO based gate dielectrics [15]. The device with the ferroelectric gate insulator exhibits anticlockwise hysteresis and a Vt shift opposed to the threshold voltage. This behavior is evidence for a switchable dipole in the gate insulator (Fig. 7) and in agreement with the observation of ferroelectricity in MIM capacitors. Ferrolectric switching was observed in devices with gate dielectrics as thin as 5.5 nm. Fig. 8 shows the threshold voltage shift of such in a devices in dependence of polarity and bias for 1s pulses. At high negative programming bias, charge trapping from the channel overcompensates the V_t shift from the dipole. Therefore, -3V and 4V were chosen as programming bias for further evidence. Fig. 9 shows the programming behavior of devices at different compositions. A clear crossover from dipole switching for FE to charge trapping for AFE insulators is evident.

The threshold voltage shift in FE devices was retained in unbiased state, allowing the non-volatile storage of information. Extrapolation to 10 years yields a memory window of 650 mV (Fig. 10), which suggests the viability of long-term data storage. We note that this is an exceptionally long retention time for a FEFET which usually suffer from retention time loss due to imperfect interfaces to silicon.

To test the lateral scalability limits of this technology, we also manufactured short channel devices. Functional devices were observed down to 80 nm x 150 nm (WxL), the smallest structure on the mask set (Fig. 11, Fig. 7).

Conclusions

We reported the formation of ferroelectric o-HfO_2 in thin films and manufactured functional nano-scale FeFETs with promising electrical characteristics. Both lateral dimensions and dielectric thickness are at least an order of magnitude smaller than previously reported devices with conventional ferroelectrics (Fig. 12).

Both the extraordinary reduction in size and the improvement in device characteristics are driven by the vastly superior material properties in this application and suggest the viability of nano-scale FeFET memory based on FE-HfO_2.

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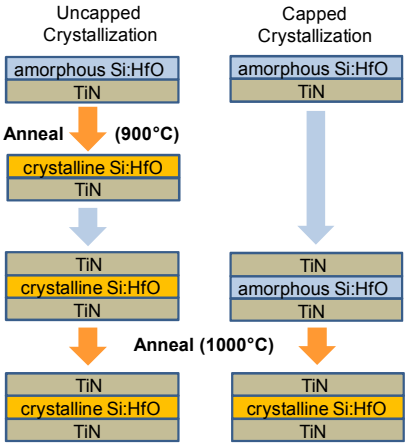

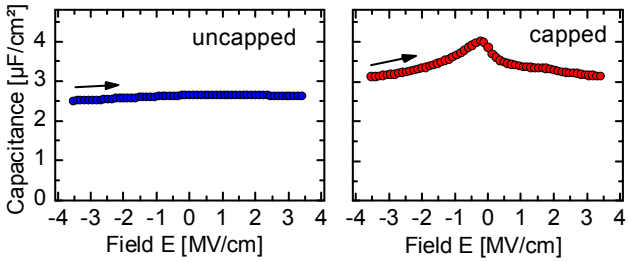

Figure 1 (left) Process flows for the manufacturing of HfSiO (10 nm) based metal-insulator-metal (MIM) capacitors with crystallization before and after top electrode deposition. (above) Small signal capacitance-voltage sweeps. If crystallization is induced after capping, nonlinear C-V characteristics are observed.

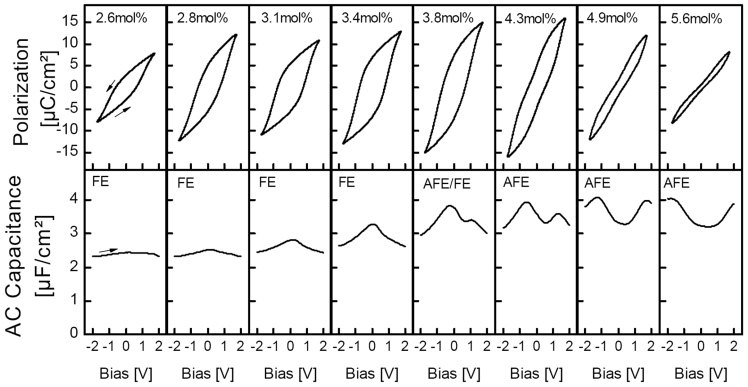

Figure 2 Polarization- and Capacitance-Voltage sweeps of a series of capped HfSiO (8.5nm) MIM-Capacitors. A gradual transition from ferroelectric to antiferroelectric polarization curves is observed. This is reflected in the C-V curves as a transition from one to two peaks.

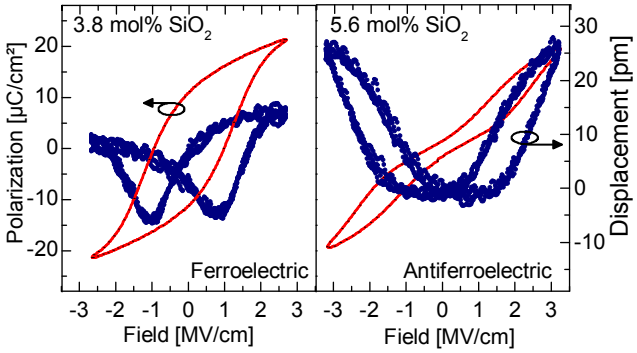

Figure 3 Polarization and piezoelectric displacement measurements (double beam laser interferometer) of MIM capacitor samples with ferroelectric and antiferroelectric HfSiO insulators.

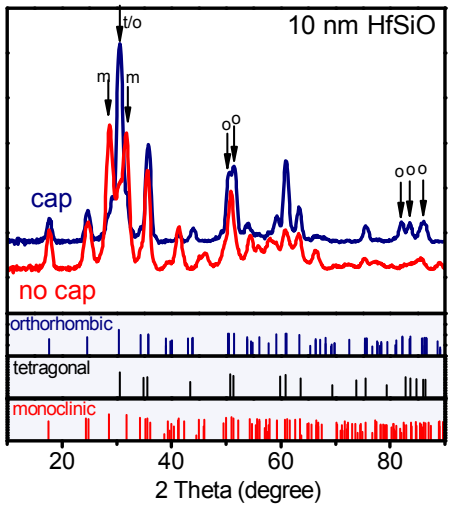

Figure 4 Grazing incidence X-ray diffraction measurements of two HfSiO samples of the same composition where crystallization was induced with and without capping. The molar SiO_2 content is approximately 3%, a composition where ferroelectricity was observed in MIM capacitors. The uncapped sample shows a diffraction pattern typical for a tetragonal/monoclinic phase mixture. The capped sample diffractions which can be assigned to an orthorhombic phase with space group $Pbc2_1$

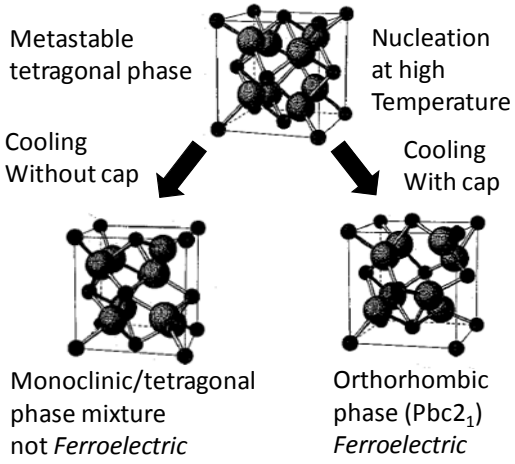

Figure 5 Formation of the orthorhombic phase proceeds by transformation from the tetragonal phase during cooling. Crystallization is induced by high temperature annealing. If the film is not capped, a partial transformation into the monoclinic phase occurs. In the presence of a mechanical cap, a transformation into the orthorhombic phase occurs instead.

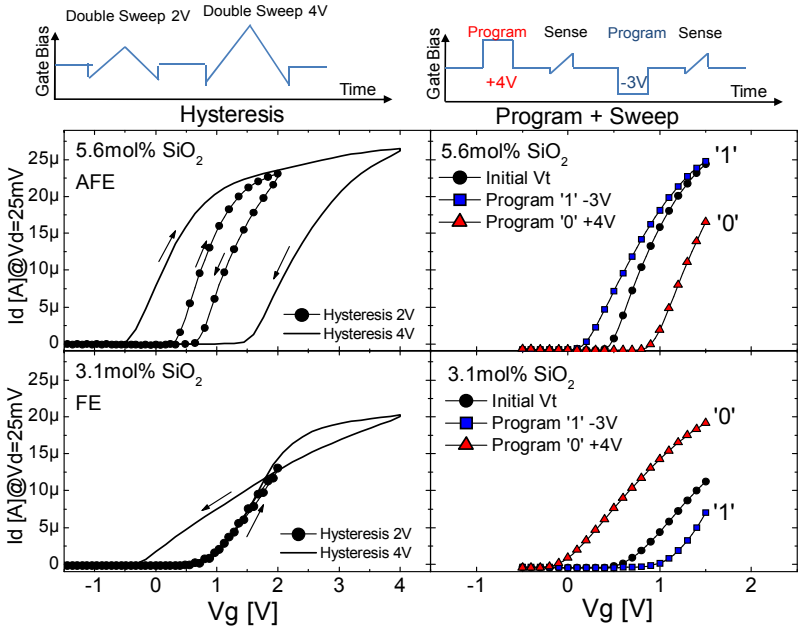

Figure 6 Characterization of transistors with gate dielectrics that showed antiferroelectric (top row) and ferroelectric (bottom row) behavior in capacitors. The left column shows the drain current for a double sweep of the gate voltage. The right column shows gate-voltage sweeps for devices that were programmed with discrete pulses of 1s (limited by prober).

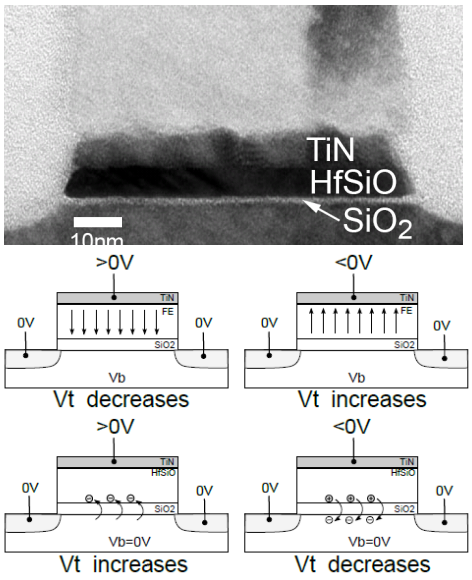

Figure 7 Top: transmission electron microscopy cross section of a short-channel transistor with FE-HfSiO. Bottom: schematic representation of charge carrier trapping and dipole switching leading to opposed Vt shifts.

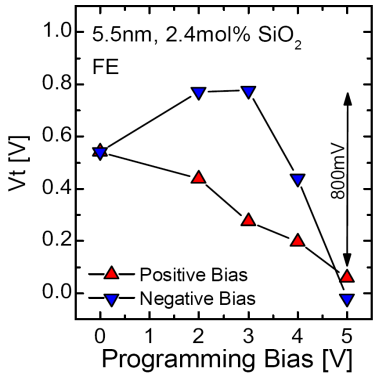

Figure 8 Programming of a FeFET (100µm x 20µm) with 5.5 nm gate insulator thickness. Trapping compensates the threshold voltage shift for negative programming bias above 3V, leading to a reduction of the memory window.

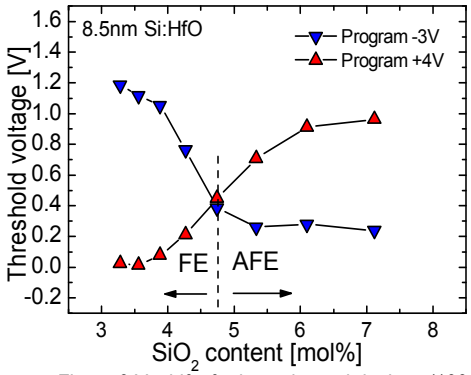

Figure 9 Vt shifts for long channel devices (100µm x 20µm) with different gate insulator compositions. Devices with FE gate insulator shift opposed to the programming voltage, while charge trapping in the AFE regime leads to a threshold voltage shift into the same direction.

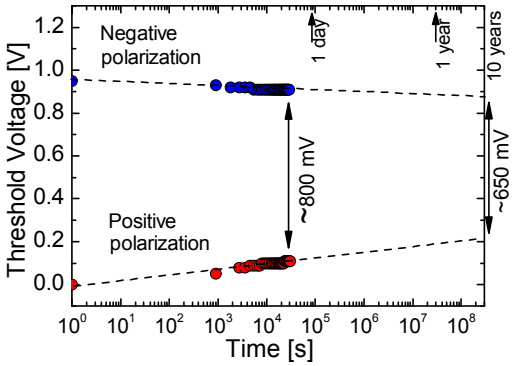

Figure 10 Data retention characteristics of a long channel device (100µm x 20µm) with 3% HfSiO. The threshold voltage was read out by gate bias sweeps every 15 minutes. All terminals were grounded between measurements

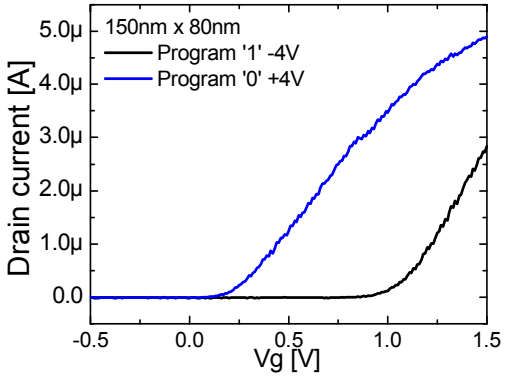

Figure 11 demonstration of the successful programming of a short channel device with dimensions 150 nm x 80 nm and 7nm gate insulator thickness, the smallest device on the mask set.

	SBT FeFET	PZT FeFET	This work
Gate Stack	Pt/SBT/HfAlO	Al/PZT/Dy_2O_3	TiN/HfSiO/SiO_2
FE/IF Thickness	400 nm/10 nm	250 nm/20 nm	**8.5 nm/1.2 nm (5.5 nm/1.2 nm)**
Thermal budget	800°C	700°C	1000°C
Memory Window	400 mV	800 mV	1000 mV
10y Memory Window	250 mV	?	650 mV
Programming Voltage	-6V/+6V	-8V/8V	-3V/4V

Figure 12 Comparison of FE-HfSiO based field effect transistors to, in our knowledge, the best previously published devices based on conventional ferroelectrics SBT and PZT [3].